S. No.	Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
								Sessional	Final Exam	Total
6	ECE-612	Verilog HDL Programming Lab	PCC	1	0	0	2	50	-	50

Course Outcomes:

At the end of the course the student will be able to:	
CO1	Develop design flow for the given application using VLSI tools
CO2	Interpret CMOS technology circuits with their specifications.
CO3	Use relevant Verilog HDL model for given application.
CO4	Analyze Verilog HDL program for the given circuits.
CO5	Implement the combinational & sequential logic circuits using Verilog HDL.

List of Experiments of Verilog HDL Programming Lab:

S. No.	Experiments
1	Write a Verilog code to realize all the logic gates
2	Write Verilog codes for the following combinational designs
	a. 3:8 decoder
	b. 4: 1 Multiplexer
	c. parity generator
	d. 4 Bit comparator
	e. 4 bit binary to gray converter
	f. Write a Verilog code to describe the functions of a Full Adder using three modeling styles
3	Write Verilog code to model RS & JK Flip flop
4	Write Verilog code for 4 Bit Up / Down Counter
5	Write Verilog program for 8 bit shift register
6	Write a Verilog program to implement a 4 digit seven segment display
7	Write a Verilog code to model 32 bit ALU
8	Miscellaneous