



Kot Bhalwal, Jammu



Model Institute of Engineering
& Technology (Autonomous)
Course Handout

COURSE HANDOUT

MICROPROCESSORS (COM-503)

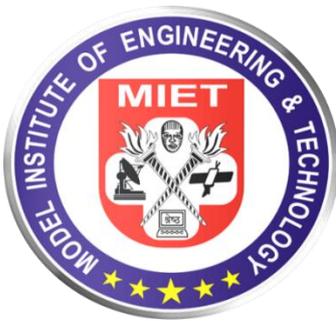
CSE-5TH SEMESTER

ACADEMIC YEAR (2024-25)

Ms. Gurpreet Kour Sodhi & Ms. Shiveta Bhat

Assistant Professor

Department of Electronics and Communication Engineering



IET
FUTURE BEGINS HERE....

Department of Computer Science Engineering

Model Institute of Engineering & Technology (Autonomous)

Kot Bhalwal, Jammu - 181122

www.mietjmu.in



Dr. Arun K. Gupta Teaching-Learning Centre

Version 1.1



Please Do Not Print Unless Necessary



Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
COM 503	Microprocessors	PCC	4	3	1	0	50	100	150

COURSE OUTCOMES

At the end of the course the student will be able to:	
CO1	Appreciate the architectural elements in a Microprocessor and their functionality.
CO2	Analyze, design, implement and test various assembly language programs of moderate complexity.
CO3	Classify the instruction set of 8085 and 8086 microprocessors and distinguish the use of different and apply them in assembly level programming.
CO4	Appreciate the evolution of RISC and ARM processors and the improvements over older microprocessor
CO5	Appraise the architecture of advanced processor families

Unit-I

Architecture of 8085: Block diagram, Pin Description of 8085, Instruction Set and Instruction Format, Addressing Modes, Looping, Counting and Indexing. 8085 Interrupts, Interrupt handling in 8085, Enabling, disabling and masking of interrupts. (8 Hrs)

Unit-II

Programmable Interface Devices: - Basics of Programmable I/O, General Purpose Programmable Peripheral Devices – 8255A, 8259A, Direct Memory Access Controller – 8237 (12 Hours)

Unit-III

Architecture of 8086: Memory Address space and data organization, segment registers and memory segmentation, generating memory addresses, IO address space, addressing modes, Minimum mode and Maximum mode. (8 Hours)

Unit-IV

RISC Processors and ARM: The RISC revolution, RISC Architecture and its characteristics, Pipeline bubbles, accessing external memory in RISC systems, Reducing the branch penalties, Branch prediction, ARM processors, ARM registers, ARM instructions, The ARM built-in shift mechanism, ARM branch instructions, sequence control, Data movement and memory reference instructions. (12 Hours)

Unit-V:

Advanced Microprocessors: Concept of core processor. Basic features of Advanced Microprocessors - Pentium - I3, I5 and I7. (8 Hours)

Textbooks

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Microprocessor Architecture, Programming, and Applications with the 8085	R.S. Ganorkar	Penram International	5 th (2011)
2.	Microprocessor Theory and Applications with 68000/68020 and Pentium	Mohamed Rafiquzzaman, Wiley-Interscience	Wiley-Interscience	1 st (2009)



Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Experiments in Microprocessors and Interfacing: Programming and Hardware	D V hall,	McGraw Hill	2nd (1992)
2	Advanced Microprocessor And Interfacing	B Ram	McGraw-Hill Education Europe	1 st (2017)
3	Microprocessor and Programmed Logic	Kenneth Short	Pearson Education	1 st (1980)

COURSE PLAN		
Unit-I Architecture of 8085		
S.No	Topics	Recommended Books
1	Block Diagram	Book 1, Ch.2
2	Pin Description of 8085	Book 1, Ch.2
3	Instruction Set and Instruction Format	Book 1, Ch.6
4	Addressing Modes	Book 1, Ch.6
5	Looping, counting and Indexing	Book 1, Ch.7
6	8085 Interrupts	Book 1, Ch.12
7.	Interrupt handling in 8085	Book 1, Ch.12
8	Enabling, disabling and masking of interrupts	Book 1, Ch.12
Unit-II Programmable Interface Devices		
9	Basics of Programmable I/O	Book 1, Ch.14
10	General Purpose Programmable Peripheral Devices – 8255A	Book 1, Ch.14
11	8259A	Book 1, Ch.14
12	Direct Memory Access Controller – 8237	Book 1, Ch.14
Unit-III Architecture of 8086		
13	Memory Address space and data organization	Book 2, Ch.2
14	segment registers and memory segmentation	Book 2, Ch.2
15	generating memory addresses.	Book 2, Ch.2
16	IO address space, addressing modes	Book 2, Ch.2
17	Minimum mode and Maximum mode.	Book 2, Ch.2
Unit-IV RISC Processors and ARM		
18	The RISC revolution	Book 2, Ch.3
19	RISC Architecture and its characteristics	Book 2, Ch.3
20	Pipeline bubbles	Book 2, Ch.3
21	accessing external memory in RISC systems	Book 2, Ch.3
22	Reducing the branch penalties	Book 2, Ch.3
23	Branch prediction	Book 2, Ch.3
24	ARM processors	Book 2, Ch.4
25	ARM registers	Book 2, Ch.4
26	ARM instructions	Book 2, Ch.4



27	The ARM built-in shift mechanism	Book 2, Ch.4
28	ARM branch instructions	Book 2, Ch.4
29	Sequence control	Book 2, Ch.4
30	Data movement and memory reference instructions	Book 2, Ch.4
Unit-V Advanced Microprocessors		
31	Concept of core processor	Book 2, Ch.5
32	Basic features of Advanced Microprocessors - Pentium - I3, I5 and I7.	Book 2, Ch.5

ADDITIONAL WEB RESOURCES

1	NPTEL: Course on Microprocessors and Interfacing by Prof. Shaik Rafi Ahamed of IIT Guwahati https://onlinecourses.nptel.ac.in/noc20_ee11/preview
2	NPTEL: Course on Microprocessor and Microcontroller by Prof. Santanu Chattopadhyay of IIT Kharagpur https://onlinecourses.nptel.ac.in/noc20_ee42/preview

GRADING AND ASSESSMENT

- **Sessional Test:** 20 marks
- **Assignment:** 20 marks
- **Attendance:** 10 marks
- **Final Examination:** 100 marks

COURSE POLICIES

- **Attendance:** Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity:** MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions:** Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**
Monday (01:00 PM - 01:40 PM)
Friday (01:00 PM - 01:40 PM)
- **Contact Information**
shiveta.ece@mietjammu.in
gurpreetsodhi.ece@mietjammu.in