



Kot Bhalwal, Jammu



Model Institute of Engineering  
& Technology (Autonomous)  
Course Handout

## COURSE HANDOUT

DIGITAL ELETRONICS (ECE-302)

ECE 3<sup>rd</sup> SEMESTER

ACADEMIC YEAR (2024-25)

**Dr. Surbhi Sharma**

Assistant Professor

Department of Electronics & Communication Engineering



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Dr. Arun K. Gupta Teaching-Learning Centre

Version 1.1



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**SYLLABUS**

Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
ECE-302	Digital Electronics	Core	4	3	1	0	50	100	150

**COURSE OUTCOMES**

At the end of the course the student will be able to:	
CO1	Understand and examine various number systems to be used in digital design.
CO2	Minimize the expressions using Karnaugh map method and implement them using logic gates.
CO3	Design and analyze various combinational and sequential circuits.
CO4	Understand and analyze various analog and digital converters.
CO5	Formulate problems and simplify with state minimizing techniques.

**Section-A**

**Unit 1:** Data and number systems: Binary, Octal and Hexadecimal representation and their conversions; BCD, ASCII, EBDIC, Gray codes, Excess-3 and their conversions; Signed and unsigned binary number representation with 1's and 2's complement methods, Binary arithmetic, Overview of Boolean algebra, Simplification of logic variable using K-map method, Quine McCluskey method.

(12 Hrs)

**Unit 2:** Combinational circuits: Encoder, Decoder, Comparator, Binary Adder-Subtractor, Parallel Adder, Multiplexer, De-Multiplexer, Code converters and Parity Generator and checker, Memory Systems: RAM, ROM, EPROM, EEROM, Design of combinational circuits-using ROM, Programming logic devices and gate arrays (PLAs and PLDs).

(12 Hrs)

**Unit 3:** Sequential Circuits: Basic memory elements, S-R, J-K (master-slave), D and T Flip-Flops, their conversions with excitation table. Various types of Registers, Synchronous and Asynchronous Counters and their design. State Machine Design, State machine as a sequential controller, Moore and Mealy state machines.

(12 Hrs)

**Section-B**

**Unit 4:** Analog and Digital Converters: Different types of A/D (flash, successive approximation, delta encoded) and D/A(R-2RLadderandbinaryweighted) conversion techniques.

(6 Hrs)

**Unit 5:** Logic Families: TTL, ECL, MOS and CMOS, their operation and specifications.

(4 Hrs)

**Text Books**

S.No.	Name of the Books	Author	Publisher Name	Edition (Pub. yr.)
1	Modern Digital Electronics	R.P. Jain	McGraw-Hill	4 <sup>th</sup> (2010)
2	Fundamentals of Digital Circuits	Anand Kumar	PHI	4 <sup>th</sup> (2016)
3	Digital Design	M. Morris Mano	Pearson	3 <sup>rd</sup> (2012)

**Reference Books**

S.No.	Name of the Books	Author	Publisher Name	Edition (Pub. Yr.)
1	Digital Electronics	A.K. Maini	Wiley India	1 <sup>st</sup> (2007)
2	Digital Electronics	Kharate	Oxford	1 <sup>st</sup> (2012)





**COURSE PLAN**

<b>Unit-I Data and Number Systems</b>		
<b>S.No</b>	<b>Topics</b>	<b>Recommended Books</b>
1	Binary numbers, Number –Base Conversions Arithmetic operations using Number system	Book 1, Ch.2
2	Data Representation –fixed and floating, Complements (1’s and 2’s)	Book 1, Ch.2
3	Binary codes –weighted/non-weighted codes, BCD codes, Excess 3 code, grey codes, Conversion between codes	Book 1, Ch.2
4	Code convertors Codes for error detection and correction (Hamming code)	Book 2, Ch.1
5	Karnaugh Map (upto five variables), Quine Mc-clusky Methods	Book 1, Ch.5
<b>Unit-II Combinational Circuits</b>		
6	Combinational Logic design -Half and Full adders, Half and full Subtractor	Book 1, Ch.7
7	BCD Adder, Comparators	Book 2, Ch.7
8	Decoders, Encoders, Multiplexers, De-Multiplexers	Book 1, Ch.7
9	Programmed logic devices–Read only memory	Book 1, Ch.12
10	Programmable Read only Memories (PROM)	Book 1, Ch.12
11	Programmable Logic Arrays (PLA) and Programmable Array Logic (PAL)	Book 2, Ch.12
<b>Unit- III Sequential Circuits</b>		
12	Latches and Flip-flops, conversion between flip flops	Book 2, Ch.10
13	Shift Registers	Book 2, Ch.11
14	Synchronous and Asynchronous counters	Book 2, Ch.12
15	State Machine Design and sequential controller.	Book 2, Ch.14
16	Moore and Mealy state machines	Book 2, Ch.14
<b>Unit-IV Analog and Digital Converters</b>		
17	Different types of A/D (flash, successive approximation)	Book 2, Ch.17
18	Different types of A/D (delta encoded)	Book 2, Ch.17
19	Different types of D/A(R-2RLadder)	Book 2, Ch.17
20	Different types of D/A (Binary weighted)	Book 2, Ch.17
<b>Unit-V Logic Families</b>		
21	TTL and ECL	Book 1, Ch.16
22	MOS and CMOS.	Book 1, Ch.16
23	Operation and specifications.	Book 1, Ch.16

**ADDITIONAL WEB RESOURCES**

1.	<p><b>NPTEL:</b> Video lectures</p> <p>1 <a href="https://www.digimat.in/nptel/courses/video/108105132/L01.html">https://www.digimat.in/nptel/courses/video/108105132/L01.html</a> Number Systems</p> <p>2. <a href="https://nptel.ac.in/courses/106/102/106102181/">https://nptel.ac.in/courses/106/102/106102181/</a> Basic of digital circuits pdf</p> <p>2 <a href="https://nptel.ac.in/courses/108105132">https://nptel.ac.in/courses/108105132</a> Sequential Circuits</p> <p>3 <a href="https://nptel.ac.in/courses/108105113">https://nptel.ac.in/courses/108105113</a> Boolean Algebra</p> <p>4 <a href="https://nptel.ac.in/courses/108105117">https://nptel.ac.in/courses/108105117</a> Multiplexer</p> <p>5 <a href="https://nptel.ac.in/courses/106/102/106102181/">https://nptel.ac.in/courses/106/102/106102181/</a> Realization using K-Maps</p>
2.	<p><b>VLAB LINK:</b> Digital electronics</p> <p><a href="https://de-iitr.vlabs.ac.in/List%20of%20experiments.html">https://de-iitr.vlabs.ac.in/List%20of%20experiments.html</a></p> <p><a href="http://vlabs.iitkgp.ernet.in/dec/exp5/index.html#">http://vlabs.iitkgp.ernet.in/dec/exp5/index.html#</a></p> <p><a href="http://vlabs.iitkgp.ernet.in/dec/exp9/index.html#">http://vlabs.iitkgp.ernet.in/dec/exp9/index.html#</a></p>



### GRADING AND ASSESSMENT

- **Sessional Test:** 20 marks
- **Assignment:** 20 marks
- **Attendance:** 10 marks
- **Final Examination:** 100 marks

### COURSE POLICIES

- **Attendance:** Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity:** MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions:** Assignments and projects must be submitted by the specified timelines.

### FACULTY INFORMATION

- **Office Hours**  
Tuesday (12:55 PM – 01:45 PM)
- **Contact Information**  
[surbhi.ece@mietjammu.in](mailto:surbhi.ece@mietjammu.in)