COURSE HANDOUT

Computer Organization and Architecture (COM-301)

B.E-3rd SEMESTER

ACADEMIC YEAR (2024-25)

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Department of CSE

Model Institute of Engineering & Technology (Autonomous)

KotBhalwal, Jammu - 181122

www.mietjmu.in

Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
COM-301	Computer Organization and Architecture	PCC	5	3	2	0	50	100	150

Course Outcomes

At the end of the course the student will be able to	
CO1	Understand the structure, including logical and functional components of a computer.
CO2	Illustrate various elementary concepts of computer architecture including syntax of register transfer language, micro-operations, instruction cycle, and control unit.
CO3	Develop understanding of techniques involved in the computer arithmetic operations.
CO4	Comprehend various instruction formats and addressing modes.
CO5	Articulate the concept of pipelining, multiprocessors, and input-output organization.

Detailed Syllabus

Section-A

Unit 1: Introduction: Overview of Digital Fundamentals.

(5 Hrs)

Unit 2: Register Transfer and Micro operation: Register Transfer Language, Register Transfer, Bus and Memory Transfer, Arithmetic Micro operations, Logic Micro operations and Shift, Micro operations.

(10 Hrs)

Unit 3: Basic Computer Organization and Design: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory Reference Instructions, Input-Output Interrupts, Design of Basic Computer, Design of Accumulator Logic.

(10 Hrs)

Section-B

Unit 4: Micro-programmed Control Unit: Control Memory, Address Sequencing. Central Processing Unit: Introduction, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes. Computer Arithmetic Introduction, Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating Point Arithmetic Operation, Decimal Arithmetic Unit, Decimal Arithmetic Operations.

(12 Hrs)

Unit 5: Peripheral devices, Input - Output interface, Asynchronous Data Transfer, Modes of Data Transfer, Priority Interrupt, Direct Memory Access, Input - Output Processor. Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware, Flynn's classification of parallel processing systems, pipelining concepts.

(12 Hrs)

Text Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Computer System and Architecture	Mano, Morris	Pearson Education	3rd (2017)

Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
2	Computer Organization and Architecture	Stallings, William	Pearson Education	10th (2016)
3	Computer Organization	Carl Hamacher, Zvonko Vranesic, Safwat Zaky	McGraw Hill Education	6th (2011)

COURSE PLAN		
Unit-I Overview of Digital Fundamentals		
S.No	**Topics**	**Recommended Books**
1	Overview of Digital Electronics	Book 1,Ch 1
2	Basics of Computer Organization and Architecture	Book 1,Ch 3
3	Number System	Book 1,Ch 3
4	Logic Gates	Book 1,Ch 1
5	Complement	Book 1,Ch 3
Unit-II Register Transfer and Microoperation		
8	Register Transfer and Register transfer Language	Book 1,Ch 4
9	Register Transfer Operations	Book 1,Ch 4
10	Bus Transfer and Memory Transfer	Book 1,Ch 4
11	Arithmetic Microoperations	Book 1,Ch 4
12	Logic Micro Operation	Book 1,Ch 4
13	Shift microoperation	Book 1,Ch 4
Unit-III Basic Computer Organization and Design		
14	Instruction Code	Book 1,Ch 5
15	Computer Registers	Book 1,Ch 5
16	Computer Instructions	Book 1,Ch 5
17	Timing and Control Signals	Book 1,Ch 5
18	Instruction Cycle	Book 1,Ch 5
19	Memory Reference Instructions	Book 1,Ch 5
20	Input-Output Interrupts	Book 1,Ch 5
21	Design of Basic Computer	Book 1,Ch 5
22	Design of Accumulator Logic.	Book 1,Ch 5
Unit-IV Micro-programmed Control Unit		
23	Control Memory, Address Sequencing. Central Processing Unit	Book 1,Ch 7
24	General Register Organization, Stack Organization, Instruction Formats	Book 1,Ch 7
25	Addressing Modes. Computer Arithmetic Introduction, Addition and Subtraction	Book 1,Ch 10
26	Multiplication Algorithms, Division Algorithms	Book 1,Ch 10
27	Floating Point Arithmetic Operation, Decimal Arithmetic Unit, Decimal Arithmetic Operations	Book 1,Ch 10
Unit-V Peripheral devices		
28	Input - Output interface	Book 1,Ch 11
29	Asynchronous Data Transfer	Book 1,Ch 11
30	Modes of Data Transfer	Book 1,Ch 11
31	Priority Interrupt	Book 1,Ch 11
32	Direct Memory Access	Book 1,Ch 11
32	Input - Output Processor	Book 1,Ch 11
34	Memory Hierarchy,Main Memory,Auxiliary Memory,Associative Memory,Cache Memory,	Book 1,Ch 12
35	Virtual Memory, Memory Management Hardware	Book 1,Ch 12
36	Flynn's classification of parallel processing systems,	Book 1,Ch 9

ADDITIONAL WEB RESOURCES

1.	**Coursera courses**: Computer and Peripheral Hardware https://www.coursera.org/learn/illinois-tech-computer-and-peripheral-hardware
2.	Udemy:Computer Organization & Architecture https://www.udemy.com/course/computer-organization-and-architecture-j/?couponCode=ST4MT73124

GRADING AND ASSESSMENT

- **Sessional Test**: 20 marks
- **Assignment**: 10 marks
- **Attendance**: 10 marks
- **Final Examination**: 100 marks

COURSE POLICIES

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**

Monday (12:05 PM - 12:55 PM)
Friday (12:05 PM - 12:55 PM)

- **Contact Information**

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