COURSE HANDOUT

Computer Architecture & VLSI Design (MCA-103)

MCA-1ST SEMESTER

ACADEMIC YEAR (2024-25)

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Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
MCA-103	Computer Architecture & VLSI Design	PCC	4	4	0	0	40	60	100

COURSE OUTCOMES

At the end of the course the student will be able to:	
CO1	Understand components of digital electronics, logical organization and the computer arithmetic.
CO2	Minimize the expressions using Karnaugh map method and implement them using Logic Gates.
CO3	Design and analyze various combinational and sequential circuits
CO4	Understand the organization and structure of computer memory.
CO5	Understand the basic parts of a VHDL model

Section-A

UNIT–I: Digital Systems and Number Representation: Von Neumann architecture, digital and analog systems. Number system, their types & conversions; Decimal, Binary, Octal, Hexadecimal; Binary Arithmetic: Binary arithmetic operations, Representation of negative numbers; 1's complement and 2's complement, Code Representation: BCD code & Excess-3 and their rules of arithmetic operations.

(10 Hrs)

UNIT–2: Logic Gates and Boolean algebra: AND, OR, NOT, NAND, XOR, NOR, XNOR gates, Boolean laws and their Expressions. Representation in SOP, POS form and their simplifications, K–map, code converters, Error detection &correction: Hamming code.

(10 Hrs)

UNIT–3: Combinational and sequential Circuits : Half & Full adders & subtractors, parallel adders, encoder, decoder, Multiplexer De-Multiplexer, Flip-flops and their types, level clocking and edge triggered clocking, Registers and their types, bi-directional register.

(10 Hrs)

Section-B

UNIT–4: Memories and bus structure: Basic memory cell, Memory hierarchy, characteristics, memory types and accessing techniques, static and dynamic Memory, cache memory. Memory address map to CPU, bus structure, memory-mapped and I/O mapped technique, Modes of I/O transfers, instruction & interrupt life cycle.

(10 Hrs)

UNIT –5: VHDL components and tools: Introduction to VHDL, need and importance of VHDL, characteristics, basic components of VHDL -entities, architectures, configuration, package, library, simple VHDL program. Understanding tools and environments– GHDL VHDL simulator, Xilinx ISE (FPGA synthesis tool set), IMAGE simulation accelerator (FPGA based co-simulation environment).

(10 Hrs)

Textbooks

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Fundamentals of Digital Circuits	Anand Kumar	PHI	4th (2016)
2.	Digital Electronics	A. K. Maini	Wiley India	1st (2007)
3.	Digital Electronics	Kharate	Oxford	1st (2012)

Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Digital Design	M. Morris Mano	Pearson	5th (2012)
2	Computer System Architecture	M. M. Mano	Pearson	3rd (2012)

COURSE PLAN		
Unit-I Digital Systems and Number Representation		
S.No	**Topics**	**Recommended Books**
1	Von Neumann architecture	Book 1, Ch.1
2	digital and analog systems	Book 1, Ch.1
3	Number system, their types & conversions; Decimal, Binary	Book 1, Ch 2
4	Octal, Hexadecimal	Book 1, Ch.2
5	Binary Arithmetic: Binary arithmetic operations	Book 1, Ch.2
6	Representation of negative numbers; 1's complement and 2's complement	Book 2, Ch.2
7	Code Representation: BCD code & Excess-3 and their rules of arithmetic operations.	Book 1, Ch.3
Unit-II Logic Gates and Boolean algebra		
8	AND, OR, NOT, NAND, XOR, NOR, XNOR gates	Book 1, Ch.5
9	Boolean laws and their Expressions.	Book 1, Ch.5
10	Representation in SOP, POS form and their simplifications	Book 1, Ch.6
11	K–map	Book 2, Ch.6
12	code converters	Book 1, Ch.7
13	Error detection & correction: Hamming code.	Book 1, Ch.3
Unit-III Combinational and sequential Circuits		
14	Half & Full adders & subtractors	Book 1, Ch7
15	parallel adders	Book 1, Ch.7
16	Encoder, decoder	Book 1, Ch.7
17	Multiplexer De-Multiplexer	Book 1, Ch.7
18	Flip-flops and their types	Book 2, Ch.10
19	level clocking and edge triggered clocking	Book 2, Ch.10
20	Registers and their types	Book 1, Ch.9
21	bi-directional register	Book 1, Ch.9
Unit-IV Memories and bus structure		
22	Basic memory cell, Memory hierarchy, characteristics	Book 2, Ch.12(reference book)
23	memory types and accessing techniques	Book 2, Ch.12(reference book)
24	static and dynamic Memory, cache memory	Book 2, Ch.12(reference book)
25	Memory address map to CPU	Book 2, Ch.12(reference book)
26	bus structure	Book 2, Ch.11(reference book)
27	memory-mapped and I/O mapped technique	Book 2, Ch.11(reference book)

28	Modes of I/O transfers	Book 2, Ch.11(reference book)
29	instruction & interrupt life cycle	Book 2, Ch.11(reference book)
Unit-V VHDL components and tools		
30	Introduction to VHDL, need and importance of VHDL	https://www.ee.iitb.ac.in/~smdp/DKStutorials/vhdl-overview.pdf
31	characteristics, basic components of VHDL	https://www.ee.iitb.ac.in/~smdp/DKStutorials/vhdl-overview.pdf
32	entities, architectures, configuration, package	https://www.ee.iitb.ac.in/~smdp/DKStutorials/vhdl-overview.pdf
33	library, simple VHDL program	https://www.ee.iitb.ac.in/~smdp/DKStutorials/vhdl-overview.pdf
34	Understanding tools and environments– GHDL VHDL simulator	https://youtu.be/PEViqQ_1i1c?si=PEZ6fqVCq_iHK36T
35	Xilinx ISE (FPGA synthesis tool set)	https://youtu.be/PEViqQ_1i1c?si=PEZ6fqVCq_iHK36T
36	IMAGE simulation accelerator (FPGA based co-simulation environment)	https://youtu.be/mwJ3uMWvJX0?si=AooRsp2bOfXZZn-Q

ADDITIONAL WEB RESOURCES

1.	VHDL Tutorial by Peter J. Ashenden https://www.eecs.umich.edu/courses/doing_dsp/handout/vhdl-tutorial.pdf
2.	**NPTEL:** Video lectures on digital circuits by Prof. Santanu Chattopadhyaya, IIT Kharagpur https://youtu.be/PEViqQ_1i1c?si=PEZ6fqVCq_iHK36T

GRADING AND ASSESSMENT

- **Sessional Test**: 20 marks
- **Assignment**: 10 marks
- **Attendance**: 10 marks
- **Final Examination**: 60 marks

COURSE POLICIES

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**

  Monday (12:05 PM - 12:55 PM)
  Friday (12:05 PM - 12:55 PM)

- **Contact Information**
  archana.bca@mietjammu.in