# COURSE HANDOUT

COMPUTER ORGANIZATION (BCAMJ-302)

BCA (HONS)-3RD SEMESTER

ACADEMIC YEAR (2024-25)

**Ms. Amita Khanna**

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| Course Code | Course Name | Course Type | Cd | L | T | P | Marks | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Sessional | Final Exam | Total |
| BCAMJ-302 | Computer Organization | Major | 4 | 4 | 0 | 0 | **20** | **60** | 100 |

**COURSE OUTCOMES**

| At the end of the course the student will be able to: | |
|---|---|
| CO1 | Analyze the logic expressions using Boolean algebra principles, logic gates, and truth tables. |
| CO2 | Implement basic combinational circuits to solve digital logic problems. |
| CO3 | Describe the operation and characteristics of Sequential Circuits. |
| CO4 | Explain the key components of computer organization and to understand their role in computer system. |
| CO5 | Describe the various types of memory and their roles in the memory hierarchy. |

**Unit-I**

Introduction to Boolean algebra -Addition and Multiplication in Boolean algebra: Binary logic function, Logic gates and Truth tables; AND logic, OR logic, NOT logic, NAND logic, NOR logic, EX-OR logic, EX-NOR logic, Boolean rules and Laws, De-Morgan's theorem, Simplification of logic variable using K-map method.

(10 Hours)

**Unit-II**

Combinational Circuits: Introduction, Encoder, Decoder, Comparator, Half Adder, Full Adder, Half Subtractor, Full Subtractor Multiplexer and De-Multiplexer, Truth Tables, Circuit Diagram ,functions and implementation

(8 Hours)

**Unit-III**

Sequential Circuits: D Flip Flop, SR Flip Flop, JK Flip Flop Circuit Diagram, JK Flip Flop Truth Table, JK Flip Flop, Race around condition, Master Slave JK Flip Flop, T Flip Flop, Register, Shift Registers(SISO,SIPO,PISO,PIPO), Bi-Directional Shift Register, Counters.

(10 Hours)

**Unit- lV**

Basic computer organization and design: Instruction codes, Stored Program Organization, Indirect Address, Computer Registers, Common bus system, computer instruction, timing and control, Instruction Cycle, input-output and interrupt, design of computer.

(8 Hours)

**Unit-V**

Memory System: Memory Hierarchy, Main Memory, RAM ROM Chips, Memory Address Map, Organization of RAM, SRAM, DRAM, Read only memory ROM-EROM, EEPROM, Auxiliary Memory, Associative Memory, Cache Memory, Virtual memory.

(8 Hours)

**Textbooks**

| S.No | Name of the Books | Name of the Author | Publisher Name | Edition (Pub.Yr.) |
|---|---|---|---|---|
| 1 | Computer Organization and Architecture | Mano, Morris | Pearson Education | 3rd(2017) |
| 2. | Digital Design | Mark Gardener | Pearson Education | 6th(2018) |

**Reference Books**

| S.No | Name of the Books | Name of the Author | Publisher Name | Edition (Pub.Yr.) |
|---|---|---|---|---|
| 1 | Computer Organization and Architecture | Stallings, William | Pearson Publishing | 11th(2022) |

| COURSE PLAN | | |
|---|---|---|
| **Unit-I Introduction to Boolean Algebra** | | |
| **S.No** | **Topics** | **Recommended Books** |
| 1 | Addition and Multiplication in Boolean Algebra | Book 2, Ch.1 |
| 2 | Logic Gates and Truth Tables | Book 2, Ch.1 |
| 3 | Boolean Rules and Laws | Book 1, Ch.2 |
| 4 | De-Morgan's Theorem | Book 2, Ch.2 |
| 5 | Simplification of Logical Variables | Book 2, Ch.2 |
| 6 | SOP Form | Book 2, Ch.2 |
| 7 | POS Form | Book 2, Ch.2 |
| **Unit-II Combinational Circuits** | | |
| 8 | Encoders | Book 1, Ch.2 |
| 9 | Decoders | Book 1, Ch.3 |
| 10 | Comparator | Book 2, Ch.3 |
| 11 | Adders | Book 2, Ch.4 |
| 12 | Subtractors | Book 2, Ch.4 |
| 13 | Multiplexers | Book 2, Ch.4 |
| 14 | De-multiplexers | Book 2, Ch.4 |
| **Unit-III Sequential Circuits** | | |
| 15 | D Flip Flop | Book 2, Ch.4 |
| 16 | SR Flip Flop | Book 2, Ch.4 |
| 17 | JK Flip Flop | Book 2, Ch.4 |
| 18 | T Flip Flop | Book 2, Ch.5 |
| 19 | Registers | Book 2, Ch.5 |
| 20 | Shift Register and Bi-directional Shift Register | Book 2, Ch.5 |
| 21 | Counters | Book 1, Ch.11 |
| **Unit-IV Basic Computer Organization and Design** | | |
| 22 | Instruction Codes | Book 2, Ch.12 |
| 23 | Stored program Organization | Book 1, Ch.8 |
| 24 | Indirect Address | Book 1, Ch.8 |
| 25 | Computer Registers | Book 1, Ch.8 |
| 26 | Common Bus system | Book 1, Ch.8 |
| 27 | Computer Instructions | Book 1, Ch.8 |
| 28 | I/o Interrupt | Book 1, Ch.8 |
| **Unit-V Memory System** | | |
| 29 | Design of Computer | Book 1, Ch.7 |
| 30 | RAM/ROM Chips | Book 1, Ch.7 |
| 31 | Memory Address Map | Book 2, Ch.7 |
| 32 | Organization of RAM | Book 1, Ch.7 |
| 33 | Read Only Memory | Book 1, Ch.7 |
| 34 | Auxiliary Memory | Book1, Ch. 7 |
| 35 | Associative Memory | Book 2,Ch 7 |
| 36 | Cache Memory | Book 2, Ch.7 |
| 37 | Virtual Memory | Book 2, Ch.7 |

**ADDITIONAL WEB RESOURCES**

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|---|---|
| 1. | **MOOC:** Computer Organization https://www.coursera.org/specializations/learn/jisuanji-zucheng?source=search |
| 2. | **NPTEL:** Video lectures on Computer Organization Lecture Series by Dr. Rajiv Misra, Professor, IIT Patna https://onlinecourses.nptel.ac.in/noc24_cs130/preview |

**GRADING AND ASSESSMENT**

- **Sessional Test**: 20 marks
- **Assignment**: 10 marks
- **Attendance**: 10marks
- **Final Examination**: 60 marks

**COURSE POLICIES**

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

**FACULTY INFORMATION**

- **Office Hours**

  Monday (01:45 PM – 02:35 PM)
  Friday (01:45 PM – 02:35 PM)

- **Contact Information**
  amita.bca@mietjammu.in