COURSE HANDOUT

VLSI Circuit Design (ECE-602)
ECE-6TH SEMESTER

ACADEMIC YEAR (2023-24)

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Department of ECE

Electronics and Communication Engineering

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Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
ECE-602	VLSI Circuit Design	Core	4	3	1	0	50	100	150

COURSE OUTCOMES

At the end of the course the student will be able to:	
CO1	Describe fundamentals of the VLSI circuit Design using Verilog HDL.
CO2	Recognize the Verilog HDL, contents, syntax of programming for the CMOS circuits.
CO3	Classify the combinational & sequential circuits using Verilog HDL.
CO4	Verify the simulation techniques and test bench creation.
CO5	Design any combinational & sequential logic circuits using Verilog HDL.

Section-A

Unit-I

Introduction to MOSFET: Basics structure and operation of MOS, MOS Symbol, MOS device design equations, MOS I-V characteristics, MOS Transistor as a Switch, Device Capacitances

(10 Hours)

Unit-II

CMOS Logic: CMOS Inverter, DC characteristics, Beta ratio effects, Combinational Logic, the NAND gate, the NOR gate, compound gates, Pass Transistor and Transmission Gate.

(10 Hours)

Unit-III

Hardware Description Languages: Data Types, Structure of Verilog Module, Operators, Types of descriptions, simulation and synthesis. Comparison of VHDL and Verilog.

(8 Hours)

Section-B

Unit- IV

Gate level and Data-flow Modeling: Verilog Gate primitives, Delay specification, rise, fall and turn-off delays, Data-flow Modeling, assignment statement, operators, operands, operator types

(16 Hours)

Unit-V

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, loops statements

(8 Hours)

Textbooks

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	CMOS Digital Integrated Circuits	Sung Ms Kang, Yusuf Lablebici	Tata McGraw Hill	4th (2018)
2.	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H.E. Weste, David Harris, Ayan Banerjee	Pearson	4th (2015)

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
3	A Verilog HDL primer	J. Bhaskar	BSP	3rd (2016)
4	A Guide to Digital Design and Synthesis	S. Palnitkar	Prentice Hall	2nd (2003)

Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Verilog Digital System Design	Z. Navabi	McGraw-Hill	2nd (2017)
2	CMOS Circuit Design, Layout and Simulation	Jacob Backer	Wiley	3rd (2010)

COURSE PLAN		
Unit-I Introduction to MOSFET		
S.No	**Topics**	**Recommended Books**
1	Basics structure and operation of MOS	Book 2, Ch.1
2	MOS Symbol	Book 2, Ch.1
3	MOS device design equations	Book 2, Ch.1
4	MOS I-V characteristics	Book 2, Ch.2
5	MOS Transistor as a Switch	Book 2, Ch.2
6	Device Capacitances	Book 2, Ch.2
Unit-II CMOS Logic		
8	CMOS Inverter	Book 2, Ch.2
9	DC characteristics	Book 2, Ch.2
10	Beta ratio effects	Book 2, Ch.1
11	Combinational Logic	Book 2, Ch.2
12	the NAND gate	Book 2, Ch.2
13	the NOR gate, compound gate	Book 2, Ch.2
14	Pass Transistor	Book 2, Ch.2
15	Transmission Gate	Book 2, Ch.2
Unit-III Hardware Description Languages		
16	Data Types	Book 4, Ch.2
17	Structure of Verilog Module	Book 4, Ch.2
18	Operators	Book 4, Ch.2
19	Types of descriptions	Book 4, Ch.2
20	Simulation and synthesis.	Book 4, Ch.2
21	Comparison of VHDL and Verilog	Book 4, Ch.2
Unit-IV Gate level and Data-flow Modeling		
22	Verilog Gate primitives	Book 4, Ch.3
23	Delay specification, rise, fall and turn-off delays,	Book 4, Ch.4
24	Data-flow Modeling	Book 4, Ch.4
25	Assignment statement	Book 4, Ch.3
26	Operators	Book 4, Ch.3
27	Operands	Book 4, Ch.3

28	Operator types	Book 4, Ch.3
Unit-V Behavioral Modeling		
29	Structured procedures	Book 4, Ch.8
30	Initial and always	Book 4, Ch.8
31	Blocking and non-blocking statements	Book 4, Ch.8
32	Delay control, generate statement,	Book 4, Ch.8
33	Event control,	Book 4, Ch.8
34	Conditional statements, loops statements	Book 4, Ch. 8
35	Loops statements	http://classweb.ece.umd.edu/enee359a/verilog_tutorial.pdf

ADDITIONAL WEB RESOURCES

1.	**MOOC:** VLSI Physical Design with Timing Analysis https://onlinecourses.nptel.ac.in/noc24_ee77/preview
2.	**NPTEL:** Video lectures on Digital System Design with PLDs and FPGAs, by Prof. Kuruvilla Varghese, IISc Bangalore. https://nptel.ac.in/courses/117/108/117108040/

GRADING AND ASSESSMENT

- **Sessional Test**: 20 marks
- **Assignment**: 20 marks
- **Attendance**: 10 marks
- **Final Examination**: 100 marks

COURSE POLICIES

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**

  Monday (12:05 PM - 12:55 PM)
  Friday (12:05 PM - 12:55 PM)

- **Contact Information**
  sarabdeep.ece@mietjammu.in