COURSE HANDOUT

VLSI CIRCUIT DESIGN (ECE-602)

ECE-6TH SEMESTER

ACADEMIC YEAR (2024-25)

Dr. Surbhi Sharma

Assistant Professor

Department of ECE

Electronics and Communication Engineering

Model Institute of Engineering & Technology (Autonomous)

Kot Bhalwal, Jammu - 181122

www.mietjmu.in

Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
ECE-602	VLSI Circuit Design	Core	4	3	1	0	50	100	150

COURSE OUTCOMES

At the end of the course the student will be able to:	
CO1	Understand the fundamentals of the MOSFET and its performance analysis .
CO2	Design and analyze complex combinational circuits using the concepts of CMOS logic.
CO3	Classify various fabrication steps used in IC fabrication. .
CO4	Recognize the Verilog HDL, contents, syntax of programming for the CMOS circuits.
CO5	Design of digital circuits using Verilog HDL.

Section-A

Unit 1: Introduction to MOSFET: Basics structure and operation of MOS, MOS Symbol, MOS device design equations, MOS I-V characteristics, MOS Transistor as a Switch, Device Capacitances

(10 Hrs)

Unit 2: CMOS Logic: CMOS Inverter, DC characteristics, Beta ratio effects, Combinational Logic, the NAND gate, the NOR gate, compound gates, Pass Transistor and Transmission Gate.

(10 Hrs)

Unit 3: Fabrication using CMOS technology: NMOS fabrication and CMOS fabrication using N-Well, P-Well & Twin- Tub processes. Layout design Rules.

(12 Hrs)

Section-B

Unit 4: Hardware Description Languages: Evaluation of CAD tools, Comparison of VHDL and Verilog. Importance of Verilog HDL. Introduction to Operators, Number specifications, Identifiers and Keywords, Modules and ports. Different types of modeling: Gate level, Data-flow and Behavioral Modeling.

(11 Hrs)

Unit5: Verilog HDLs coding: logic gates, 2-to-4-line decoder, 4 to 1 multiplexer, half adder, full adder, half subtractor, full subtractor, 4-bit adder, 4-bit gray to 4-bit binary converter and 2-bit comparator.

(9 Hrs)

Textbooks

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	CMOS Digital Integrated Circuits	Sung Ms Kang, Yusuf Lablebici	Tata McGraw Hill	4th (2018)
2.	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H.E. Weste, David Harris, Ayan Banerjee	Pearson	4th (2015)
3	A Verilog HDL primer	J. Bhaskar	BSP	3rd (2016)
4	A Guide to Digital Design and Synthesis	S. Palnitkar	Prentice Hall	2nd (2003)

Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Verilog Digital System Design	Z. Navabi	McGraw-Hill	2nd (2017)
2	CMOS Circuit Design, Layout and Simulation	Jacob Backer	Wiley	3rd (2010)

COURSE PLAN	
Unit-I Introduction to MOSFET	
S.No	**Topics**	**Recommended Books**

S.No	Topics	Recommended Books
1	Basics structure and operation of MOS	Book 1, Ch.3
2	Energy Band Diagram of MOS structure	Book 1, Ch.3
3	MOS device design equations	Book 1, Ch.3
4	Process of formation of Inversion layer	Book 1, Ch.3
5	MOS Symbol and Working of MOSFET	Book 1, Ch.3
6	MOS device design equations	Book 1, Ch.3
7	Calculation of Threshold Voltage	Book 1, Ch.3
8	MOS I-V characteristics	Book 1, Ch.3
9	MOS Transistor as a Switch	Book 1, Ch.3
10	Device Capacitances	Book 1, Ch.3
Unit-II CMOS Logic		
11	Concept of Inverter Design	Book 1, Ch.5
12	CMOS Inverter	Book 1, Ch.5
13	DC characteristics and Voltage Analysis	Book 1, Ch.5
14	Symmetric Inverter, Beta ratio effects	Book 1, Ch.5
15	Combinational Logic	Book 1, Ch.7
16	NAND gate	Book 1, Ch.7
17	NOR gate, compound gate	Book 1, Ch.7
18	Concept of Pass Transistor	Book 1, Ch.7
19	Concept of Transmission gates	Book 1, Ch.7
20	Logic design using Transmission Gate	Book 1, Ch.7
Unit-III CMOS Fabrication Technology		
21	VLSI Design Flow- Front-end & Back-end design	Book 1, Ch.1
22	Y-Chart details	Book 1, Ch.1
23	Concept of Fabrication and processes involved	Book 1, Ch.1
24	NMOS Fabrication	Book 1, Ch.2
25	CMOS Fabrication	Book 1, Ch.2
26	Concept of P-Well and N-well	Book 1, Ch.2
27	Circuit Design using CMOS Technology	Book 1, Ch.2
28	Stick Diagram Concept	Book 1, Ch.2
29	Layout Design Rules	Book 1, Ch.2
30	Desing the Layout of CMOS and basic gate	Book 1, Ch.2
Unit-IV Hardware Description Languages		
31	Comparison of VHDL and Verilog	Book 4, Ch.2
32	Types of descriptions	Book 4, Ch.2
33	Simulation and synthesis.	Book 4, Ch.2
34	Data Types, Modules and Ports	Book 4, Ch.2
35	Structure of Verilog Module and VHDL Module	Book 4, Ch.2
36	Introduction to Operators	Book 4, Ch.2
37	Identifiers and Keywords	Book 4, Ch.3

38	Gate-level Modeling	Book 4, Ch.4
39	Data-flow Modeling	Book 4, Ch.4
40	Behavioral Modeling	Book 4, Ch.3
41	Assignment statement	
Unit-V Verilog HDL Coding		
42	Verilog design for Basic Gates	Book 4, Ch.8
43	Verilog design for Half Adder and Full Adder	Book 4, Ch.8
44	Verilog design for Half and Full Subtractor	Book 4, Ch.8
45	Verilog design for Multiplexer with different modelling styles	Book 4, Ch.8
46	Verilog design for Encoder and decoder with different modelling styles	Book 4, Ch.8
47	Verilog design for Gray to Binary code converters	Book 4, Ch. 8
48	Verilog design for Binary to BCD code converters	Book 4, Ch.8
49	Verilog design for 2-Bit comparator	Book 4, Ch.8

1.	**MOOC:** VLSI Physical Design with Timing Analysis https://onlinecourses.nptel.ac.in/noc24_ee77/preview
2.	**NPTEL:** Video lectures on Digital System Design with PLDs and FPGAs, by Prof. Kuruvilla Varghese, IISc Bangalore. https://nptel.ac.in/courses/117/108/117108040/

GRADING AND ASSESSMENT

- **Sessional Test**: 20 marks
- **Assignment**: 20 marks
- **Attendance**: 10 marks
- **Final Examination**: 100 marks

COURSE POLICIES

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**

  Wednesday (12:55 PM – 1:45 PM)
  Friday (2:35 PM – 3:25 PM)

- **Contact Information**
  surbhi.ece@mietjammu.in

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