COURSE HANDOUT

MODERN COMPUTER ARCHITECTURE (COM-401)

BE-IVTH SEMESTER

ACADEMIC YEAR (2024-25)

Dr. Mir Aadil

Assistant Professor

Department of Computer Science & Engineering

Department of Computer Science & Engineering

Model Institute of Engineering & Technology (Autonomous)

Kot Bhalwal, Jammu - 181122

www.mietjmu.in

Course Code	Course Name	Course Type	Cd	L	T	P	Marks		
							Sessional	Final Exam	Total
COM-401	**Modern Computer Architecture**	Core	4		0	0	50	100	150

COURSE OUTCOMES

At the end of the course the student will be able to:	
CO1	Describe the building blocks of modern microprocessors and advanced computing systems.
CO2	Appraise advanced memory management architectures and optimization techniques.
CO3	Analyse the design of Pipelined and Multiprocessors systems in distributed computing.
CO4	Appreciate the various communication and synchronization mechanisms used in modern computing.
CO5	Analyze diverse high-performance computing architectures and models.

Unit-I

Basics Designing combinational and sequential logic, computers registers and instructions, timing, and control, instructions cycle, memory reference instruction, I/O interruption, Adder and Subtractor circuits, Booth Multiplication Algorithm, Pipelining Review, control hazards and the motivation for caches, cache characteristics and basic High-Performance Computing with CUDA Programming.

(5 Hours)

Unit-II

Multi-core Architecture Memory technologies, hierarchical memory systems, the locality principle and caching, direct mapped caches, block size, cache conflicts, associative caches, write strategies, advanced optimisations, performance improvement techniques.

(9 Hours)

Unit-III

Distributed Computing Systems and Concurrency Relation to Parallel Multiprocessors/multicomputer Systems, Distributed and Concurrent Programs, Message Passing vs. Shared Memory Systems, Synchronous vs. Asynchronous Executions, Design Issues and Challenges.

(10 Hours)

Unit- IV

Distributed Computing Technologies, Clocks and Synchronization, Coordination and Agreement Algorithms, Global State and Distributed Transactions

(5 Hours)

Unit-V

High Performance Computing (HPC), HPC Architecture, Parallel Processing, Parallel Memory Models, Data vs Task Parallelism, High Throughput Computing, Vectorization, Multithreading.

(8 Hours)

Textbooks

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Computer System & Architecture	M. Morris Mano	Prentice Hall of India	3rd (2017)
2.	Parallel Computer Architecture: A Hardware/Software Approach	David Culler and J.P. Singh, Anoop Gupta	Morgan Kaufmann	1st (1998)

Reference Books

S.No	Name of the Books	Name of the Author	Publisher Name	Edition (Pub.Yr.)
1	Advanced Computer Architecture	Smruti R Sarangi	McGraw Hill Education (India) Private Limited	1st (2021)

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COURSE PLAN	
Unit-I	

S.No	Topics	Recommended Books
1	Basics Designing combinational and sequential logic	Book 1, Ch.1
2	Computers registers and instructions	Book 1, Ch.1
3	Instructions cycle	Book 1, Ch.1
4	Memory reference instruction	Book 2, Ch.2
5	I/O interruption	Book 2, Ch.2
6	Adder circuits (Half Adder, Full Adder)	Book 2, Ch.2
7	Subtractor circuits (Half Subtractor, Full Subtractor)	
8	Booth Multiplication Algorithm	Book 2, Ch.2
9	Pipelining Review	Book 2, Ch.2
10	control hazards and the motivation for caches	Book 2, Ch.2
11	cache characteristics	
12	Basic High-Performance Computing with CUDA Programming	Book 2, Ch.2
Unit-II		
13	Multi-core Architecture Memory technologies	Book 1, Ch.2
14	hierarchical memory systems	Book 1, Ch.2
15	locality principle and caching	Book 1, Ch.1
16	direct mapped caches	Book 2, Ch.2
17	block size, cache conflicts	Book 2, Ch.2
18	associative caches, write strategies	Book 2, Ch.2
19	advanced optimizations	Book 2, Ch.2
20	performance improvement techniques	Book 2, Ch.2
Unit-III		
21	Distributed Computing Systems	Book 2, Ch.2
22	Concurrency Relation to Parallel Multiprocessors/multicomputer Systems	
23	Distributed and Concurrent Programs,	Book 2, Ch.2
24	Message Passing vs. Shared Memory Systems	Book 2, Ch.2
25	Synchronous,	
26	Asynchronous Executions,	
27	Design Issues and Challenges	Book 2, Ch.2
Unit-IV		
28	Distributed Computing Technologies,	Book 2, Ch.3

29	Clocks and Synchronization	Book 1, Ch.4
30	Coordination and Agreement Algorithms,	Book 1, Ch.4
31	Global State	Book 2, Ch.3
32	Distributed Transactions	Book 1, Ch.3
Unit-V		
33	High Performance Computing,	Book 2, Ch.8
34	HPC Architecture	Book 1, Ch.8
35	HPC, Parallel Processing	Book 2, Ch.8
36	Parallel Memory Models	Book 2, Ch.8
37	Data vs. Task Parallelism	Book 1, Ch.8
38	High Throughput Computing	Book 2, Ch.8
39	Vectorization	Book2, Ch. 8
40	Multithreading	Book2, Ch. 8

ADDITIONAL WEB RESOURCES

1.	**NPTEL:** Multi-Core Computer Architecture https://onlinecourses.nptel.ac.in/noc23_cs113/preview

GRADING AND ASSESSMENT

- **Sessional Test**: 20 marks
- **Assignment**: 20 marks
- **Attendance**: 10 marks
- **Final Examination**: 100 marks

COURSE POLICIES

- **Attendance**: Minimum 75% attendance is mandatory to appear in the final examination of the course.
- **Academic Integrity**: MIET's academic integrity policies apply. Plagiarism will not be tolerated.
- **Late Submissions**: Assignments and projects must be submitted by the specified timelines.

FACULTY INFORMATION

- **Office Hours**

  Monday (12:05 PM - 12:55 PM)
  Friday (12:05 PM - 12:55 PM)

- **Contact Information**
  aadil.cse@mietjammu.in

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